IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

MEDIATEK, INC.,	§	
	§	
Plaintiff,	§	
	§	
vs.	§	**CASE NO. 605 CV 323**
	§	**PATENT CASE**
SANYO ELECTRIC CO LTD.; SANYO NORTH AMERICA, INC.; AND SANYO NORTH AMERICAN CORPORATION,	§	
	§	
	§	
Defendants.	§	

MEMORANDUM OPINION

This Memorandum Opinion construes disputed terms in U.S. Patent Nos. 5,751,356 ("the '356 patent"); 5,867,819 ("the '819 patent"); and 6,118,486 ("the '486 patent").

BACKGROUND

MediaTek alleges that Sanyo infringes three of its patents. The '356 patent discloses a video/audio signal coding system and method that perform multiplexing operations with a decreased processor load. The processor load is reduced by inputting video header information directly from the video encoding means for creating the video header information—as opposed to extracting the video header information from a bit stream. '356 Patent col. 2:64-3:1-4. The '819 patent discloses an inexpensive audio decoder that performs down mixing processes using a reduced memory capacity. The '486 patent discloses an apparatus and method for video signal processing in a digital television.

APPLICABLE LAW

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312

(Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). In claim construction, courts examine the patent's intrinsic evidence to define the patented invention's scope. *See id.*; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). This intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. *Phillips*, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give

a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the patentee's lexicography governs. *Id*. Also, the specification may resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. But, "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. *Home Diagnostics, Inc., v. Lifescan, Inc.*, 381 F.3d 1352, 1356 (Fed. Cir. 2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

Although extrinsic evidence can be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition is entirely unhelpful to a court. *Id*. Generally, extrinsic evidence is "less reliable than the patent and

its prosecution history in determining how to read claim terms." *Id*.

The patents in suit also contain means-plus-function limitations that require construction. Where a claim limitation is expressed in "means plus function" language and does not recite definite structure in support of its function, the limitation is subject to 35 U.S.C. § 112, ¶ 6. *Braun Med., Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). In relevant part, 35 U.S.C. § 112, ¶ 6 mandates that "such a claim limitation 'be construed to cover the corresponding structure . . . described in the specification and equivalents thereof.'" *Id*. (citing 35 U.S.C. § 112, ¶ 6). Accordingly, when faced with means-plus-function limitations, courts "must turn to the written description of the patent to find the structure that corresponds to the means recited in the [limitations]." *Id*.

Construing a means-plus-function limitation involves multiple inquiries. "The first step in construing [a means-plus-function] limitation is a determination of the function of the means-plus-function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). Once a court has determined the limitation's function, "the next step is to determine the corresponding structure disclosed in the specification and equivalents thereof." *Id*. A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id*. Moreover, the focus of the "corresponding structure" inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id*.

THE '356 PATENT[1]

Video encoding means

The parties agree this term is subject to 35 U.S.C. § 112, ¶ 6 and that the claimed function is "encoding a video signal into video data, attaching encoding information to said video data to generate encoded video data, and generating data number information indicative of a number of the encoded video data corresponding to a predetermined video data unit."

The corresponding structure is "a video signal encoder including an encoder circuit utilizing an MPEG standard, a header creation circuit, and a multiplexer circuit; and equivalents."

MediaTek argues that the corresponding structure should be "a video signal encoder including an encoder circuit, a header creation circuit, and a multiplexer circuit; a video signal encoder including an encoder circuit utilizing the MPEG standard, a header creation circuit, and a multiplexer circuit; and equivalents." The Court disagrees with MediaTek that the structure covers any encoder circuit; the structure is limited to an encoder circuit utilizing an MPEG standard because this is the only structure disclosed in the patent. *See Medtronic, Inc.*, 248 F.3d at 1311; '356 Patent col. 3:39-41; 3:52-54; 3:60-64; 4:14-30; 4:63-65.

Sanyo argues that the structure is limited to an encoder circuit implementing the MPEG1 or MPEG2 standard. Sanyo asserts the patent only discloses these standards because these were the only MPEG standards existing at the time of filing and because the subsequent MPEG4 is too dissimilar to be characterized as part of an evolving standard. The Court disagrees. The specification does not limit the structure to MPEG1 or MPEG2. '356 Patent col. 3:39-41 ("FIG. 1

[1] Appendix A contains the relevant patent claims for the three patents-at-issue with the disputed terms in bold.

[shows] an arrangement of a video/audio signal coding system according to an embodiment based on *an* MPEG system.") (emphasis added). MPEG was commonly understood to be an evolving standard because it had gone through two versions by the time of filing. Sanyo does not offer evidence of a clear disclaimer by the inventor that would limit the invention to MPEG1 or MPEG2. Furthermore, because dependent claim 3 adds MPEG1 and MPEG2 as a limitation on this term, it is presumed that this limitation is not part of the term as used in independent claim 1. *See Phillips*, 415 F.3d at 1314-15; '356 Patent col. 6:26-34; 6:62-67.

Sanyo proposes constructions for three sub-terms—"data number information," "predetermined video data unit," and "header information"—because these terms lack an ordinary and accustomed meaning. MediaTek objects and offers their own constructions that are based on the patent specification.

First, the Court construes "data number information" as "a value indicative of the bit length of a picture." Sanyo argues that data number information should be construed as "a value indicative of the bit length of a picture, which is not part of the encoded video data." Sanyo's proposed construction adds the limitation that the data number information be excluded from the encoded video data. Sanyo bases its construction on the specification's description of the header creation circuit 12 of Figure 1. *See* '356 Patent col. 4:12-25. Sanyo argues that the central purpose of the invention as shown in Figure 1 is to reduce the processor load and therefore the data number information must be excluded from the data sent to the processor. However, the specification does not support this additional limitation, which describes the header creation circuit 12 as determining the length of the bit stream. *Id.*

Next, the Court construes "predetermined video data unit" as "a predetermined set of

pictures." Sanyo argues that the sub-term should be construed as "a predetermined group of pictures (GOP) that can include one or more pictures." Sanyo attempts to limit the sub-term to GOPs, which are used in the MPEG standard. As discussed above, the structure requires an encoder circuit using an MPEG standard. Further construction of this sub-term in light of this required structure does not assist the trier of fact—it merely adds unnecessary verbiage.

Finally, the Court construes "header information" as "data that carries information about video data." Sanyo argues that the term should be construed as "data that carries information about various parts of the encoded video data which defines the beginning of the predetermined video unit." Sanyo's construction includes a predetermined video unit, and therefore only covers GOP headers. This definition improperly excludes system headers and picture headers, which are disclosed in the specification. *See* '356 Patent col. 4:20-25.

Audio encoding means

The parties agree this term is subject to 35 U.S.C. § 112, ¶ 6 and that the claimed function is "encoding an audio signal into audio data to generate encoded audio data."

The corresponding structure is "an audio signal encoder that is separate from the video signal encoder circuit and that implements audio compression according to an MPEG standard; and equivalents." MediaTek argues that the corresponding structure should be "an audio signal encoder, an audio signal encoder implementing the MPEG standard, and equivalents." The structure is limited to what the specification discloses; the specification only discusses compressed audio signals and only discloses compression accomplished according to an MPEG standard. *See Medtronic, Inc.*, 248 F.3d at 1311; '356 Patent col. 4:26-28. Nowhere does the patent disclose the processing of uncompressed audio signals. Further, the specification only discloses an audio encoding means that

is separate from the video encoding means. '356 Patent Figure 1; col. 3:41-48.

System header generating means

The parties agree this term is subject to 35 U.S.C. § 112, ¶ 6. The Court construes the function as "generating system headers on the basis of the header information and the data number information stored in the first memory." Sanyo argues that the function should be construed as "generating a complete system header based on the header information and data number information stored in the first memory without extracting the video header information from the bit stream." Sanyo argues that the specification teaches the creation of the system header in only one way:

> the processor reads the video information . . . from the memory 3 "and creates the system header information for making a layered system structure." ['356 Patent col. 4:51-54.] When the processor 4 has completed created the system header, it "writes the created system header in the header information memory 5." *Id*. at 5:10-11.

Brief for Defendants at 47 (Docket No. 150).

However, Sanyo cites no intrinsic support for including the limitation that the system header be "complete." The patent specification cited by Sanyo simply states that "[t]he processor 4 writes the created system header in the header information memory 5." '356 Patent col. 5:10-11. Sanyo's proposed requirement that the system headers be generated "without extracting the video header information from the bit stream" is an unnecessary limitation because the claim language only requires that system headers be generated "on the basis of the header information and the data number information stored in said first memory." '356 Patent col. 6:41-43. Because the claim language limits how the function must be accomplished, it is not necessary in this instance to construe the function in terms of what the claim language excludes.

The parties and the Court agree that the corresponding structure is a "processor and equivalents."

Multiplexing means

The parties do not dispute that this limitation should be construed as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6. This term appears in claims 1 and 7. The parties and the Court agree that the function for claim 1 is "multiplexing the encoded video data generated by said video encoding means, the encoded audio data generated by said audio encoding means and the system headers stored in said second memory." The parties and the Court agree that the function for claim 7 is "multiplexing the encoded video data generated by said video encoding means, the encoded audio data generated by said audio encoding means and the system headers stored in said first control means."

The Court modifies Sanyo's proposed structure and identifies the corresponding structure for the term's function in claims 1 and 7 as "a multiplexer circuit separate from the processor." Sanyo argues that the structure should be construed as "a discrete multiplexer circuit." MediaTek agreed at the hearing that the structure is limited to a "multiplexer circuit," but objected to the requirement that it be "discrete." The specification only discloses a multiplexing means that is separate from the processor; nowhere does the specification disclose the processor undertaking the multiplexing function. *See* '356 Patent col. 3:44-49; 5:23-25; 6:47-51. The structure is limited to what the specification discloses. *See Medtronic, Inc.*, 248 F.3d at 1311.

System header

The Court adopts the construction to which the parties agreed at the claim construction hearing: "a data structure that is combined with the encoded video and audio data streams."

A first control means

The parties agree this term is subject to 35 U.S.C. § 112, ¶ 6. The Court construes the

function as "temporarily storing at least the header information and the data number information generated by said video encoding means, generating system headers on the basis of the header information and the data number information, and temporarily storing the system headers."[2] The Court agrees with the parties that the corresponding structure is a "processor and equivalents."

THE '819 PATENT

Frequency domain down mixing means

The parties agree that this limitation should be construed as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6. This term appears in claims 1 and 6.

i) Claim 1

The parties and the Court agree that the function of claim 1 should be construed as "processing said frequency domain audio data so as to mix the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio."

The Court modifies Sanyo's proposal and identifies the corresponding structure as "a frequency domain down mixing circuit as shown in element 40 of Figure 7 or element 101 of Figure 8 that is constructed to implement equation (4); and equivalents." Sanyo argues that the structure must implement equation (4) and argues that the corresponding structure should be "a frequency domain down mixing circuit as shown in element 40 of Figure 7 or element 101 of Figure 8, which implements equation (4)." MediaTek argues that implementation of equation (4) is not required, and

[2] The Court's construction reiterates language in claim 7. The parties' agreed function as submitted to the Court is identical, except that the submitted function did not include the words "and the data number information." If this omission was deliberate, the parties may move for reconsideration of the Court's construction and outline why this language should be excised from the construction.

argues that the structure should be "a frequency domain down mixing circuit; a frequency domain down mixing circuit implementing equation (4); and equivalents."

Sanyo argues that equation (4) must be included because it is an algorithm that is part of the structure. *See* '819 Patent col. 9:12-14 ("The process to be executed in the frequency domain down mixing circuit 101 is described by the following equation (4)."). Sanyo further argues that equation (4) must be included because it is the only structure identified in the patent that performs the functions related to a "predetermined level ratio"—a function that Sanyo argues a generic down mixing circuit cannot perform. *See id.* at col. 9:12-26.

"In a means-plus-function claim in which the disclosed structure is a computer, or microprocessor, programmed to carry out an algorithm, the disclosed structure is not the general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm." *WMS Gaming, Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999); *see Harris Corp. v. Ericsson, Inc.*, 417 F.3d 1241, 1249 (Fed. Cir. 2005) ("The corresponding structure for a 112 ¶ 6 claim for a computer-implemented function is the algorithm disclosed in the specification.").

Sanyo argues that *WMS Gaming* requires the structure of this function to include equation (4) as the disclosed algorithm. MediaTek argues that the '819 patent does not distinguish between hardware and software implementations and that *WMS Gaming* does not apply to hardware implementations of the '819 patent because that case dealt with software. MediaTek's arguments are unconvincing.

First, a thorough reading of the patent shows that it is directed at hardware. The patent does not use "processor" or "computer" even once, while the term "circuit" appears in the patent more

than 100 times. *See generally* '819 Patent. Further, the specification refers to circuits "executing" processes. *See, e.g., id.* at col. 3:40-41 ("The IMDCT circuit 33 executes an IMDCT process."); *see also* col. 2:46; 11:36; 12:12; 12:17; 12:20. In addition, the specification uniformly uses other terminology consistent with hardware applications, including "hardware," "constructional," "construction," and "constructed." *See* '819 Patent col. 4:47 ("FIG. 6 is a hardware constructional diagram"); col. 8:1-2 ("FIG. 9 is a diagram showing a constructional example of a hardware of an audio decoder"); *see also* col. 1:31; 4:47; 7:48; 7:54; 7:59-60; 7:62; 7:65; 8:10-11; 8:15-16; 8:18-19; 8:21-22; 8:31; 8:58; 10:13-14; 10:36-46; 11:19; 11:21; 11:28-31; 12:54-57; 13:55-58; 14:33-36; 15:17-18. Here the specification uniformly refers to hardware implementations and the patent does not provide reference to a software implementation. The only structures described in the specification are circuits—i.e. hardware—constructed to implement the disclosed equations.

MediaTek argues that the structure includes both hardware and software implementations either because the patent disclosed both or, alternatively, because the patent does not distinguish between implementations. As discussed above, MediaTek's argument fails because this patent is directed at hardware implementations. Although one of ordinary skill may understand that an undisclosed software implementation is *possible*, means-plus-function claims are limited to the structure disclosed in the specification. *See Medtronic, Inc.*, 248 F.3d at 1311.

Second, the reasoning of *WMS Gaming* is applicable to this hardware means-plus-function claim. MediaTek's attempt to distinguish *WMS Gaming* solely on the basis that it dealt with software is not persuasive. *WMS Gaming* stated that a general processor becomes a special purpose machine when it is programed to perform an algorithm and held that the structure for a means-plus-function claim covering such a special-purpose computer includes both the computer and the

algorithm programmed into it. *WMS Gaming, Inc.*, 184 F.3d at 1348-39.

Here, the patent discloses hardware implementing an algorithm. MediaTek's attempt to distinguish *WMS Gaming* solely on the basis that it dealt with specialized software is not compelling. This Court has held that the structure of a non-programmable, special-purpose circuit should not be construed to include the algorithm where the specification sufficiently describes the special circuit's function. *Alt v. Medtronic, Inc*., No. 2:04-cv-370-97 slip op. at 9 (E.D. Tex. Nov. 30, 2005) (Davis, J.). Here, the specification describes the corresponding circuit's function *only* in terms of equation (4), therefore the structure for the claimed frequency domain down mixing means in claim 1 must include equation (4). *See* '819 Patent col. 9:12-14. ("The process to be executed in the frequency domain down mixing circuit is described by the following equation (4)."); *see also Harris*, 417 F.3d at 1254 (stating that "[a]spects of this algorithm can vary based on implementation, as the specification implies"); *Connectel, LLC v. Cisco Sys., Inc.*, 428 F. Supp. 2d 564, 576 (E.D. Tex. 2006) (Davis, J.) (holding that the algorithm-at-issue was not limited to the specific equations given in the specification because the specification allowed for "other permutations and variations . . . easily derived by one of skill in the art").

ii) Claim 6

The Court modifies Sanyo's proposed construction and construes the term's function in claim 6 as "processing the frequency domain audio data so as to mix the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio, eliminating the audio signal of said at least one channel from targets to be mixed." MediaTek proposes the same function for claim 6 as for claim 1. Sanyo argues that claim 6 includes an additional function and that the functional language should be included: "processing the frequency

domain audio data so as to mix the audio signals of the plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio, eliminating the audio data of channel(s) with differing conversion block lengths from the down mixing process."

Claim 6 is a dependent claim that depends on claim 3, which in turn depends on claim 1. Claim 6 states that the "said frequency domain down mixing means *eliminates the audio signal of said at least one channel from targets to be mixed*." '819 Patent col. 19:42-45 (emphasis added). MediaTek argues that while the additional language is a claim limitation, it does not affect the function of the down mixing means. This argument fails. The language describes an additional *function* that the down mixing means first claimed in claim 1 performs in dependent claim 6. *See Lockheed Martin Corp. v. Space Sys*., 249 F.3d 1314, 1324 (Fed. Cir. 2001) (stating that a function may not "be improperly broadened by ignoring the clear limitations contained in the claim language"). The Court agrees with Sanyo that this additional language describes the function. The Court modifies Sanyo's construction to track the claim language. *See* '819 Patent col. 19:42-45.

The corresponding structure for the term in claim 6 is "a frequency domain down mixing circuit as shown in element 40 of Figure 7 or element 101 of Figure 8 that is constructed to implement equation (4); and equivalents." MediaTek argues that the corresponding structure is "a frequency domain down mixing circuit; a frequency domain down mixing circuit implementing equation (4); and equivalents." For the reasons discussed above, the structure includes equation (4). Sanyo argues that the expanded function of the down mixing means in claim 6 renders the claim invalid because there is no structure that is identified for "eliminating" any channel. This argument fails. The specification identifies sufficient structure—it details how circuitry may be removed to passively eliminate channels. *See* '819 Patent col. 10:36-43 ("In order to construct a further

inexpensive audio decoder, the frequency base to time base converting circuit 105, fifth memory circuit 115, and time base to frequency base converting circuit 104 in FIG. 8 may be omitted and when the conversion block lengths among the channels do not coincide, it is sufficient to execute a process of eliminating one or more channel having a different conversion block length from the targets of the down mixing process.").

Frequency base to time base converting means

The parties agree that this limitation should be construed as a means-plus-function limitation under 35 U.S.C. § 112, ¶ 6. This limitation appears in claims 1, 3, 11, 13, and 16.

i) Claim 1

The parties and the Court agree that the function in claim 1 is "converting the frequency domain audio data processed by said frequency domain down mixing means from the frequency domain to a time domain." The Court identifies the corresponding structure as "an IMDCT circuit implementing equation (2), (5), or (6); and equivalents." MediaTek argues that the corresponding structure is "a frequency base to time base converting circuit; an IMDCT circuit; a frequency base to time base converting circuit implementing equation (2), (5), or (6); an IMDCT circuit implementing equation (2), (5), or (6); and equivalents." Sanyo argues that the structure is "an IMDCT circuit implementing equation (2); and equivalents."

The structure is limited to an IMDCT circuit because this is the only circuit identified in the specification that performs the claimed function. *See* '819 Patent Figs. 9, 12, 14, 15, 16 (all showing an IMDCT circuit as corresponding structure). The specification provides three equations for use

with an IMDCT circuit: equation (2), equation (5), and equation (6).[3] *See* '819 Patent col. 3:43-57; 15:40-59; 15:60-16:15. The functional language of claims 1, 3, 13, and 16 may be satisfied by an IMDCT circuit implementing any of the three equations. *See id.* As discussed above, because the specification uses equations (2), (5), and (6)—and nothing else—to define the IMDCT circuit, those disclosed algorithms are part of the structure.

ii) Claim 3

MediaTek proposes the same function for claim 3 as for claim 1. The Court agrees with Sanyo that the clear language of claim 3 adds additional limitations on the function that are not present in claim 1. *See Lockheed*, 249 F.3d at 1324. The Court modifies Sanyo's proposal[4] and construes the function as "converting the frequency domain audio data processed by said frequency domain down mixing means from the frequency domain to the time domain on the basis of the block length information separated by said separating means."

The parties' arguments regarding the corresponding structure are identical to those for claim 1. For the reasons discussed above, the Court identifies the corresponding structure as "an IMDCT circuit implementing equation (2), (5), or (6); and equivalents." *See* '819 Patent col. 3:43-57; 15:40-59; 15:60-16:15.

iii) Claim 11

The Court modifies Sanyo's proposed construction and construes the function of claim 11 as "converting said frequency domain audio data from the frequency domain to a time domain by

[3] Equation (6) is a modification of equation (5) that is based on an assumption regarding the equation variables and use of a symmetry of the cosine function.

[4] The Court's construction is similar to Sanyo's proposed construction, but the Court's construction more closely tracks the claim language.

using a cosine function with respect to each of the audio signals of said plurality of channels, thereby forming a first set and a second set of time domain audio data having a symmetrical relation to each other derived from said cosine function." Sanyo argues that the function of claim 11 should be construed as "converting frequency domain audio data from the frequency domain to a time domain using a symmetrical cosine function with respect to each of multiple channels of audio data, resulting in two sets of time domain audio data that are symmetrical by nature." MediaTek argues that the function in claim 11 should be construed as "converting the frequency domain audio data from the frequency domain to a time domain by using a cosine function with respect to each of the audio signals of the plurality of channels."

MediaTek argues that the language in claim 11 "thereby forming a first set and a second set of time domain audio data having a symmetrical relation to each other derived from said cosine function," should not be construed as part of the function because it adds nothing substantive to the claim limitation. *See Lockheed*, 249 F.3d at 1324 (holding that "a whereby clause that merely states the results of the limitations in the claim add nothing to the substance of the claim"). The additional language after the "thereby" in claim 11 appears to add substance to the claim limitation, and therefore must be included in the function. *Id*. The additional language does not merely repeat earlier language in the claim or summarize what the claim limitation describes. *Contra* '819 Patent col. 20:54-55 (claim 13 language "thereby forming time domain audio data" merely re-states and summarizes the function of the frequency base to time base converting means). MediaTek's conclusory argument that the additional language merely introduces the results of the preceding claim limitation is not convincing, and the Court construes the function to include the limitation's

clear language.[5]

The corresponding structure is "an IMDCT circuit implementing equation (6); and equivalents." MediaTek proposes the same structure described above for all the claims. For the reasons discussed above, the structure is limited to an IMDCT circuit. Furthermore, the structure includes equation (6)[6] because this is the only description the specification provides for how the IMDCT circuit produces "a first and second set of time domain audio data having a symmetrical relation to each other derived from said cosine function." '819 Patent col. 20:30-33.

iv) Claims 13 and 16

The parties' arguments for the term in claim 16 are identical to their respective arguments for the term in claim 13. The Court agrees with MediaTek and construes the term's function in claims 13 and 16 as "converting said frequency domain audio data from the frequency domain to a time domain with respect to each of the audio signals of said plurality of channels." Sanyo argues that its proposed construction is more understandable to a jury: "converting each of the multiple channels of frequency domain audio data from frequency domain audio data to time domain audio data." MediaTek's construction tracks the claim language and is preferred for this function. *See* '819 Patent col. 20:52-54; 21:20-23; *Asyst Techs., Inc. v. Empak, Inc.,* 268 F.3d 1364, 1369 (Fed. Cir. 2001) ("The first step in construing a means-plus-function limitation is to identify the function *explicitly recited in the claim*.") (emphasis added).

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[5] The Court's construction is similar to Sanyo's proposed construction, but the Court's construction more closely tracks the claim language.

[6] Equation (5) is not included in the structure because equation (6) is a modification of equation (5) that includes certain assumptions regarding equation variables that are necessary to perform the function in claim 11. *See* '819 Patent col. 15:60-16:15. Equation (6) is more specific than equation (5) and the term's function in claim 11 is defined by equation (6). *See id.*

The parties' arguments for the corresponding structure for the term's function in claims 13 and 16 are identical to those proposed for claim 1. For the reasons discussed above, the Court identifies the corresponding structure as "an IMDCT circuit implementing equation (2), (5), or (6); and equivalents." *See* '819 Patent col. 3:43-57; 15:40-59; 15:60-16:15.

Separating means

The parties agree that this term is subject to 35 U.S.C. § 112, ¶ 6 and that the claimed function is "separating said frequency domain audio data and said block length information from said encoded data." At the hearing, the parties agreed that the structure includes "a demultiplexer or demultiplexing circuit." The Court agrees with the parties and identifies the corresponding structure as "a demultiplexer or demultiplexing circuit; and equivalents."

Down mixing means

The parties agree that this term is subject to 35 U.S.C. § 112, ¶ 6. This term appears in claims 13 and 16.

i) Claim 13

The parties have no substantive disagreement over the function of claim 13. The Court agrees with MediaTek and construes the function as "processing the time domain audio data, adding the time domain audio data stored in said buffer memory to the time domain audio data output from said window applying means thereby mixing the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio and for outputting the added time domain audio data to said buffer memory." Sanyo did not object to MediaTek's construction at the hearing, but argued that its proposed construction is more easily understood: "processing the time domain audio data and mixing multiple channels of time domain

audio data into a predetermined number of channels at a predetermined level ratio by adding down mixed time domain audio data stored in the PCM 'buffer memory' to the time domain audio data output from the 'window applying means'; then storing the down mixed time domain audio data in the same PCM 'buffer memory.'" MediaTek's construction is preferred because the parties have no substantive disagreement and MediaTek's construction tracks the claim language. *See* '819 Patent col. 20:59-67; 21:1-4; *Asyst Techs.,* 268 F.3d at 1369.

The corresponding structure is "a down mixing circuit that implements equation (3); and equivalents." MediaTek argues that the corresponding structure should be construed as "a down mixing circuit; a down mixing circuit implementing equation (3); and equivalents." For the reasons discussed above, the corresponding structure includes equation (3) because the specification describes the circuit only in terms of the algorithm. *See* '819 Patent col. 4:33-40.

ii) Claim 16

As with claim 13, the parties have no substantive dispute over the construction of the term's function in claim 16. The Court adopts MediaTek's proposed construction and construes the function as "adding the time domain audio data stored in said buffer memory to the time domain audio data output from said window applying means thereby mixing the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio and for outputting the added time domain audio data to said buffer memory." Sanyo argues that its construction is more understandable: "mixing multiple channels of time domain audio data into a predetermined number of channels at a predetermined level ratio by adding delayed data stored in the delay buffer from the window applying means to time domain audio data output from the window applying means; then storing the down mixed time domain audio data in the delay buffer

memory." MediaTek's construction is preferred because the parties have no substantive disagreement and MediaTek's construction tracks the claim language. *See* '819 Patent col. 20:59-67; 21:1-4; 22:4-11; *Asyst Techs.,* 268 F.3d at 1369.

The parties' arguments for the term's function in claim 16 and the corresponding structure are identical to those for the term in claim 13. For the reasons discussed above, the Court agrees with Sanyo and identifies the corresponding structure as "a down mixing circuit that implements equation (3); and equivalents." *See* '819 Patent col. 4:33-40.

Block length matching means

The parties agree that this term is subject to 35 U.S.C. § 112, ¶ 6. The parties agree that the function should be construed as "perform block length matching." This construction is much broader than the specific function described in claim 4: "block length matching means which operates in such a manner that when a length of data block to be processed by said frequency domain down mixing means differs with respect to the audio signals of said plurality of channels, the lengths of data blocks of the audio signals of said plurality of channels are made coincide and, after that, said data blocks are supplied to said frequency domain down mixing means." '819 Patent col. 19:8-15. However, because the parties have agreed that the function is "perform block length matching," the Court will construe it as such for the purposes of this case. The Court agrees with the parties and identifies the corresponding structure as "frequency base to time base converting circuit module and equivalents, a memory circuit module and equivalents, a time base to frequency base converting circuit module and equivalents, and/or a frequency base down mixing circuit module and equivalents."

THE '486 PATENT

Fixed frequency

The parties agreed at the claim construction hearing that this term does not require construction.

Raster clock signal

The Court modifies MediaTek's proposed construction and construes the term as "a periodic signal used to synchronize a display device in response to a program clock reference ("PCR")." MediaTek argues that the term should be construed according to its ordinary meaning—"a periodic signal used to synchronize a display device." Sanyo argues that the patent provides a special meaning for the term raster clock signal—"a signal with a nonstandard frequency easily derived in response to a PCR."

MediaTek agreed at the hearing that the raster clock signal is produced in response to a PCR. Sanyo asserts that the raster clock signal must be "nonstandard" and "easily derived" because the prosecution history and specification require minimal circuitry. Sanyo argues that using minimal circuitry leads to an "easily derived" raster clock signal. Sanyo further argues that a nonstandard signal is required because the specification only contemplates nonstandard signals.

Sanyo's arguments are unpersuasive. First, claims 1 and 2 do not require that the raster clock signal have a nonstandard frequency or be easily derived. *See* '486 Patent col. 14:7-54. Second, the specification allows—but does not limit this invention to—raster clock signals with nonstandard frequencies. '486 Patent col. 2:33-34 ("display raster signals *need not conform* to the waveforms commonly used"). The specification deals explicitly with nonstandard frequencies, but also states that "the invention contemplates the use of other native display formats and other raster frequencies."

'486 Patent col. 13:8-9. Finally, requiring the raster clock signal to be easily derived is not supported by the specification. It would instead add a vague term which would not assist the trier of fact. Sanyo argued at the hearing that "easily derived" is not vague because it means created with "minimal circuitry." This proposed construction is not helpful because "minimal circuitry" is itself vague.

Clock circuit

The Court agrees with MediaTek and construes the term according to its ordinary meaning as "a collection of electrical elements for producing clock signals." *See* IEEE 100 AUTH. DICT. OF IEEE STANDARD TERMS, 168 (7th ed. 2000). Sanyo argues that the term should be construed as "a circuit using a single voltage controlled oscillator ("VCO"), that reacts to a program clock reference ("PCR") of the input video signal to generate both the system clock and the raster clock."

Sanyo's construction adds three limitations: 1) the use of a single VCO, 2) generation of both the system and raster clocks, and 3) generation in reaction to a PCR. The second and third limitations are unnecessary because they are already limitations in claim 1. '486 Patent col. 14:25-30. Construing "clock circuit" to require these limitations would only add redundancy to the claim.

Sanyo argues that the specification only teaches—and therefore requires—the use a single VCO. Sanyo's interpretation attempts to improperly import a limitation from the specification into the claim. *See Phillips*, 415 F.3d at 1323. While the specification illustrates the use of a VCO, it does not limit the invention to any particular type of clock source. *See* '486 Patent col. 4:36-39; 13:1-4 (stating that the invention allows the use of a single clock source *"such as* a voltage controlled crystal oscillator") (emphasis added).

Frequency scaling

The Court agrees with MediaTek and construes the term as "multiplying and/or dividing a frequency by a given factor." Sanyo argues that the term should be construed as "doubling and/or dividing a given frequency by easily derived values to obtain a different frequency." Sanyo's argument is not based on the claim language. Instead, Sanyo argues again that the specification and prosecution history require minimal or simple circuitry, and therefore a contextual interpretation of the patent requires frequency scaling accomplished using "easily derived values." Finally, Sanyo argues that specification only discloses examples of frequency scaling that are consistent with using simple circuits, and that the invention "teaches away" from using the standard 74.25 MHz raster frequency, which would require relatively complex circuitry. *See* '486 Patent col. 8:18-21; 9:21-34; 12:46-52; 13:7-14.

As discussed above in the section construing raster clock signal, the importation of an "easily derived" limitation on this term is not supported. Sanyo's interpretation of "easily derived" as limiting multiplication to a factor of two results in an unsupported, overly-narrow reading of the specification and an improper limitation of the claim.

CONCLUSION

For the foregoing reasons, the Court interprets the claim language in this case in the manner set forth above. For ease of reference, the Court's claim interpretations are set forth in a table as Appendix B. The claims with the disputed terms in bold are set forth in Appendix A.

So ORDERED and SIGNED this 26th day of March, 2007.

LEONARD DAVIS
UNITED STATES DISTRICT JUDGE

APPENDIX A

U.S. PATENT NO. 5,751,356

1. A video/audio signal coding system comprising:

video encoding means for encoding a video signal into video data, attaching **encoding information** to said video data to generate encoded video data, and generating data number information indicative of a number of the encoded video data corresponding to a predetermined video data unit, said **encoding information** including header information indicative of a head of said encoded video data corresponding to the predetermined video data unit;

audio encoding means for encoding an audio signal into audio data to generate encoded audio data;

a first memory for temporarily storing at least the header information and the data number information generated by said **video encoding means** ;

system header generating means for generating **system headers** on the basis of the header information and the data number information stored in said first memory;

a second memory for temporarily storing the system headers generated by said **system header** generating means;

multiplexing means for multiplexing the encoded video data generated by said **video encoding means** , the encoded audio data generated by said **audio encoding means** and the **system headers** stored in said second memory; and

control means for judging a boundary corresponding to said predetermined video data unit in the encoded video data input from said **video encoding means** to said multiplexing means on the basis of the header information and the data number information stored in said first memory to thereby control multiplexing operation of said **multiplexing means**.

4. A video/audio signal coding method comprising the steps of:

encoding a video signal into video data, attaching **system header** to said video data to generate encoded video data, and generating data number information indicative of a number of the encoded video data corresponding to a predetermined video data unit, said **system header** including header information indicative of a head of said encoded video data corresponding to the predetermined video data unit;

encoding an audio signal into audio data to generate encoded audio data;

temporarily storing at least the header information and the data number information;

generating **system headers** on the basis of the stored header information and data number information, and temporarily storing the **system headers**; and

judging a boundary corresponding to said predetermined video data unit in the encoded video data on the basis of the stored header information and data number information to thereby multiplex the encoded video data, the encoded audio data and the stored **system headers**.

7. A video/audio signal coding system comprising:

video encoding means for encoding a video signal into video data, attaching **system header** to said video data to generate encoded video data, and generating data number information indicative of a number of the encoded video data corresponding to a predetermined video data unit, said **system header** including header information indicative of a head of said encoded video data corresponding to the predetermined video data unit;

audio encoding means for encoding an audio signal into audio data to generate encoded audio data;

a first control means for temporarily storing at least the header information and the data number information generated by said **video encoding means** , generating system headers on the basis of the header information and the data number information, and temporarily storing the system headers;

multiplexing means for multiplexing the encoded video data generated by said **video encoding means** , the encoded audio data generated by said **audio encoding means** and the system headers stored in said **first control means**; and

second control means for judging a boundary corresponding to said predetermined video data unit in the encoded video data input from said **video encoding means** to said **multiplexing means** on the basis of the header information and the data number information stored in said **first control means** to thereby control multiplexing operation of said **multiplexing means**.

U.S. PATENT NO. 5,867,819

1. An audio decoder for decoding encoded data including frequency domain audio data which represents audio signals of a plurality of channels in a frequency domain through a time base to frequency base conversion, comprising:

frequency domain down mixing means for processing said frequency domain audio data so as to mix the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio; and

frequency base to time base converting means for converting the frequency domain audio data processed by said **frequency domain down mixing means** from the frequency domain to a time domain.

2. A decoder according to claim 1, wherein:

said frequency domain audio data includes sample data each having a variable bit length and indicative of a sample with respect to one of the audio signals of said plurality of channels; and

said audio decoder further comprises **inverse quantizing means** for identifying the sample data by obtaining a bit length of each sample data from said frequency domain audio data and for supplying the identified sample data to said frequency domain down mixing means.

3. A decoder according to claim 1, wherein:

said frequency domain audio data has a data block of a variable length including data indicative of a variable number of samples of the audio signals of said plurality of channels;

said encoded data further includes block length information indicative of a length of each data block;

said audio decoder further comprises **separating means** for separating said frequency domain audio data and said block length information from said encoded data; and

said **frequency base to time base converting means** converts the frequency domain audio data processed by said frequency domain down mixing means from the frequency domain to the time domain on the basis of the block length information separated by said **separating means**.

4. A decoder according to claim 3, further comprising:

block length matching means which operates in such a manner that when a length of data block to be processed by said frequency domain down mixing means differs with respect to the audio signals of said plurality of channels, the lengths of data blocks of the audio signals of said plurality of channels are made coincide and, after that, said data blocks are supplied to said frequency domain down mixing means.

5. A decoder according to claim 4, wherein said block length matching means includes:

second frequency base to time base converting means which operates in such a manner that when the length of data block with respect to the audio signal of at least one channel to be processed is different from the length of data block with respect to the audio signal of the other channel to be processed, a plurality of data blocks regarding the audio signal of said at least one channel are coupled so that said plurality of coupled data blocks have a length that is equal to the length of data block with respect to the audio signal of said other channel, and the frequency domain audio data included in said plurality of coupled data blocks is converted from the frequency domain to the time domain, thereby forming time domain audio data; and

time base to frequency base converting means for forming second frequency domain audio data by converting said time domain audio data from the time domain to the frequency domain and for supplying said second frequency domain audio data to said frequency domain down mixing means.

6. A decoder according to claim 3, wherein

when the length of data block with respect to the audio signal of at least one channel to be processed is different from the length of data block with respect to the audio signal of the other channel to be processed, said **frequency domain down mixing means** eliminates the audio signal of said at least one channel from targets to be mixed.

11. An audio decoder for decoding encoded data including frequency domain audio data which represents audio signals of a plurality of channels in a frequency domain through a time base to frequency base conversion, said audio decoder comprising:

frequency base to time base converting means for converting said frequency domain audio data from the frequency domain to a time domain by using a cosine function with respect to each of the audio signals of said plurality of channels, thereby forming a first set and a second set of time domain audio data having a symmetrical relation to each other derived from said cosine function;

a buffer memory for storing only one of the first and second sets of time domain audio data;

window applying means for obtaining, from said one of the first and second sets of time domain audio data stored in said buffer memory, the other of the first and second sets of time domain audio data by using said symmetrical relation and performing a window applying arithmetic operation

13. An audio decoder for decoding encoded data including frequency domain audio data which represents audio signals of a plurality of channels in a frequency domain through a time base to frequency base conversion, said audio decoder comprising:

frequency base to time base converting means for converting said frequency domain audio data from the frequency domain to a time domain with respect to each of the audio signals of said plurality of channels, thereby forming time domain audio data;

window applying means for performing a window applying arithmetic operation for said time domain audio data;

down mixing means for processing the time domain audio data;

a buffer memory for temporarily storing the time domain audio data output from said **down mixing means**; and

said **down mixing means** for adding the time domain audio data stored in said buffer memory to the time domain audio data output from said **window applying means** thereby mixing the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio and for outputting the added time domain audio data to said buffer memory.

16. An audio decoder for decoding encoded data including frequency domain audio data which represents audio signals of a plurality of channels in a frequency domain through a time base to frequency base conversion, said audio decoder comprising:

frequency base to time base converting means for converting said frequency domain audio data from the frequency domain to a time domain with respect to each of the audio signals of said plurality of channels, thereby forming time domain audio data;

window applying means for performing a window applying arithmetic operation for said time domain audio data;

a buffer memory for delaying data which is used when said **window applying means** executes the window applying arithmetic operation; and

down mixing means for adding the time domain audio data stored in said buffer memory to the time domain audio data output from said **window applying means** thereby mixing the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio and for outputting the added time domain audio data to said buffer memory.

U.S. PATENT NO. 6,118,486

1. Apparatus for processing an input video signal having one of a plurality of **display formats** to produce an output video signal suitable for use by a display device, said display device utilizing a **fixed frequency** horizontal deflection signal and a vertical deflection signal, said apparatus comprising:

a format converter, for selectively adapting at least a horizontal **display format** of said input video signal to a horizontal **display format** defined by aid **fixed frequency** horizontal deflection signal;

a frame rate converter, coupled to said format converter, for selectively adapting a frame rate of said input video signal to a frame rate of said display device;

a raster generator, for generating, in response to a **raster clock signal**, said **fixed frequency** horizontal deflection signal and said vertical deflection signal, said vertical deflection signal having a frequency defined by a vertical **display format** of said output video signal; and

a **clock circuit**, responsive to a program clock reference (PCR) associated with said input video signal, for producing a **system clock signal** and said **raster clock signal**, said **raster clock signal** being generated by **frequency scaling** said **system clock signal**.

2. In a system for processing a video stream associated with at least one of a plurality of video **display formats**, a method for generating video and timing signals for use by a display device having a substantially fixed horizontal scanning frequency, said method comprising the steps of:

identifying a video **display format** associated with said video stream;

generating, in response to a program clock reference (PCR) associated with said video stream, a **system clock signal** and a **raster clock signal**, said **raster clock signal** being generated by **frequency scaling** said **system clock signal**;

generating, in response to the **raster clock signal**, a substantially **fixed frequency** horizontal synchronizing signal and a vertical synchronizing signal, said substantially **fixed frequency** horizontal synchronizing signal and said vertical synchronizing signal defining an active viewing area of a display device, said vertical deflection signal having a frequency defined by a vertical **display format** of said video stream; and

adapting at least a horizontal **display format** of said video stream in response to a horizontal **display format** defined by said **fixed frequency** horizontal deflection signal.

APPENDIX B

CLAIMS CONSTRUCTION FOR U.S. PATENT NO. 5,751,356

Claim Language	Court's Construction
Video encoding means Claims 1, 7	**Function:** encoding a video signal into video data, attaching encoding information to said video data to generate encoded video data, and generating data number information indicative of a number of the encoded video data corresponding to a predetermined video data unit. **Structure:** a video signal encoder including an encoder circuit utilizing an MPEG standard, a header creation circuit, and a multiplexer circuit; and equivalents. **Subterms construed:** **data number information:** a value indicative of the bit length of a picture. **predetermined video data unit:** a predetermined set of pictures. **header information:** data that carries information about video data.
Audio encoding means Claims 1, 7	**Function:** encoding an audio signal into audio data to generate encoded audio data. **Structure:** an audio signal encoder that is separate from the video signal encoder circuit and that implements audio compression according to an MPEG standard; and equivalents.
System header generating means Claim 1	**Function (claim 1):** generating system headers on the basis of the header information and the data number information stored in the first memory. **Structure:** processor and equivalents.
Multiplexing means Claims 1, 7	**Function (claim 1):** multiplexing the encoded video data generated by said video encoding means, the encoded audio data generated by said audio encoding means and the system headers stored in said second memory. **Function (claim 7):** multiplexing the encoded video data generated by said video encoding means, the encoded audio data generated by said audio encoding means and the system headers stored in said first control means. **Structure (claims 1 and 7):** a multiplexer circuit separate from the processor.
System header Claims 1, 4, and 7	a data structure that is combined with the encoded video and audio data streams.

Control means Claim 1	**Function:** judging a boundary corresponding to said predetermined video data unit in the encoded video data input from said video encoding means to said multiplexing means on the basis of the header information and the data number information stored in said first memory to thereby control multiplexing operation of said multiplexing means. **Structure:** processor and equivalents**.**
A first control means Claim 7	**Function:** temporarily storing at least the header information and the data number information generated by said video encoding means, generating system headers on the basis of the header information and the data number information, and temporarily storing the system headers. **Structure:** processor and equivalents**.**
Encoding information Claims 1, 4, and 7	information relating to video data, including header information**.**

CLAIMS CONSTRUCTION FOR U.S. PATENT NO. 5,867,819

Claim Language	Court's Construction
Frequency domain down mixing means Claims 1, 6	**Function (claim 1):** processing said frequency domain audio data so as to mix the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio. **Structure (claim 1):** a frequency domain down mixing circuit as shown in element 40 of Figure 7 or element 101 of Figure 8 that is constructed to implement equation (4); and equivalents. **Function (claim 6):** processing the frequency domain audio data so as to mix the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio, eliminating the audio signal of said at least one channel from targets to be mixed. **Structure (claim 6):** a frequency domain down mixing circuit as shown in element 40 of Figure 7 or element 101 of Figure 8 that is constructed to implement equation (4); and equivalents.

Frequency base to time base converting means Claims 1, 3, 11, 13, and 16	**Function (claim 1):** converting the frequency domain audio data processed by said frequency domain down mixing means from the frequency domain to a time domain. **Structure (claim 1):** an IMDCT circuit implementing equation (2), (5), or (6); and equivalents. **Function (claim 3):** converting the frequency domain audio data processed by said frequency domain down mixing means from the frequency domain to the time domain on the basis of the block length information separated by said separating means. **Structure (claim 3):** an IMDCT circuit implementing equation (2), (5), or (6); and equivalents. **Function (claim 11):** converting said frequency domain audio data from the frequency domain to a time domain by using a cosine function with respect to each of the audio signals of said plurality of channels, thereby forming a first set and a second set of time domain audio data having a symmetrical relation to each other derived from said cosine function. **Structure (claim 11):** an IMDCT circuit implementing equation (6); and equivalents. **Function (claims 13 and 16):** converting said frequency domain audio data from the frequency domain to a time domain with respect to each of the audio signals of said plurality of channels. **Structure (claims 13 and 16):** an IMDCT circuit implementing equation (2), (5), or (6); and equivalents.
Separating means Claim 3	**Function:** separating said frequency domain audio data and said block length information from said encoded data. **Structure:** a demultiplexer or demultiplexing circuit; and equivalents.

Down mixing means Claims 13 and 16	**Function (claim 13):** processing the time domain audio data, adding the time domain audio data stored in said buffer memory to the time domain audio data output from said window applying means thereby mixing the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio and for outputting the added time domain audio data to said buffer memory. **Function (claim 16):** adding the time domain audio data stored in said buffer memory to the time domain audio data output from said window applying means thereby mixing the audio signals of said plurality of channels into the audio signals of a predetermined number of channels at a predetermined level ratio and for outputting the added time domain audio data to said buffer memory. **Structure (claims 13 and 16):** a down mixing circuit that implements equation (3); and equivalents.
Inverse quantizing means Claim 2	**Function:** identifying the sample data by obtaining a bit length of each sample data from said frequency domain audio data and for supplying the identified sample data to said frequency domain down mixing means. **Structure:** inverse quantizing circuit or demultiplexing circuit, and equivalents.
Time base to frequency base converting means Claim 5	**Function:** forming second frequency domain audio data by converting said time domain audio data from the time domain to the frequency domain and for supplying said second frequency domain audio data to said frequency domain down mixing means. **Structure:** time base to frequency base converting circuit and equivalents.
Block length matching means Claim 4	**Function:** perform block length matching. **Structure:** frequency base to time base converting circuit module and equivalents, a memory circuit module and equivalents, a time base to frequency base converting circuit module and equivalents, and/or a frequency base down mixing circuit module and equivalents.
Window applying means Claims 11, 13, and 16	**Function (claim 11):** obtaining, from said one of the first and second sets of time domain audio data stored in said buffer memory, the other of the first and second sets of time domain audio data by using said symmetrical relation and performing a window applying arithmetic operation. **Function (claims 13 and 16):** performing a window applying arithmetic operation for said time domain audio data. **Structure (claims 11, 13, and 16):** window applying operating circuit, window applying circuit, or adding and window applying circuit, and equivalents.

CLAIMS CONSTRUCTION FOR U.S. PATENT NO. 6,118,486

Claim Language	Court's Construction
Fixed frequency Claims 1 and 2	No construction needed.
Raster clock signal Claims 1 and 2	a periodic signal used to synchronize a display device in response to a program clock reference ("PCR").
Clock circuit Claim 1	a collection of electrical elements for producing clock signals.
Frequency scaling Claims 1 and 2	multiplying and/or dividing a frequency by a given factor.
Display format Claims 1 and 2	the horizontal and vertical resolution of output visual information.
System clock signal Claims 1 and 2	a periodic signal used for timing events in a system.